Design of Polymorphic Gates Using Ambipolar Transistors

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In some situations, it would be useful to have one more logic function implemented in a digital circuit that is not needed during normal operation of the circuit but could be activated occasionally, under special circumstances. The other funtion could be a test, a watermark, an emergency function or simply any hidden secondary function you need. A conventional solution is to glue an additional circuit to the main circuitry and simply switch the output when necessary. Another approach that usually brings more efficient and smart solution could be so-called polymorphic or multifunctional electronics.

Polymorphic electronics as an approach to design and implementation of multifunctional digital circuits was proposed by team of A. Stoica at the NASA JPL about 15 years ago [1]. The main idea of polymorphic electronics is to have a single circuit that is able to exhibit more than one logic function. The function just performed by the circuit depends on the circumstances of the circuit, on a state of the environment (e.g. power supply voltage, power supply polarity, temperature, etc.). Polymorphic circuits are built from polymorphic logic gates. The change of the function of the whole circuit is caused by change of Boolean functions exhibited by employed polymorphic gates. Interconnection of polymorhic gates remains unchanged.

Main two problems of the polymorphic electronics are search for suitable polymorphic gates and synthesis methods for polymorphic circuits. The author of this presentation developed the only existing method for design of polymorphic gates based on ambipolar transistors (one of transistor types used for polymorphic gates implementation) [2]. The objective of this presentation is to formally describe the main parts of this method.

[1] A. Stoica, R. Zebulum, and D. Keymeulen, “Polymorphic electronics,” in Int. Conf. on Evolvable Systems. Springer, 2001, pp. 291–302.

[2] J. Nevoral, “Polymorfní obvody na bázi ambipolárních tranzistorů,“ In: Počítačové architektury a diagnostika PAD 2016. Bořetice: Fakulta informačních technologií VUT v Brně, 2016, pp. 45-48.