Optimal Register Allocation in Polynomial Time

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The problem of the register allocation is an important issue that has to be solved for any production-grade compiler, considering an ineffective algorithm can cause the resulting executable to run significantly slower, sometimes even by an order of magnitude.

There are many possible approaches of how to solve register allocation, and they use many different methods: integer linear programming (ILP), partitioned boolean quadratic programming (PBQP), linear scan register allocation, graph coloring. Many of these methods are NP-hard to solve, which often leads to them using heuristics instead of solving the problem optimally.

In the first part of this presentation, I will shortly explain several issues related to register allocation (particularly in CISC architectures), specifically: register aliasing, register preferences and coalescing.

The rest of the presentation will be focused on an algorithm for register allocation by Philipp Klaus Krause, which is capable of doing an optimal register allocation in polynomial time. The algorithm uses graph coloring and focuses mainly on embedded systems architectures, where it has become the default register allocator for most SDCC compiler back-ends. In this part, I will explain the basic mechanisms this algorithm uses and the results it produces.