On Complexity of Offline Partial Dynamic Reconfiguration Scheduling

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Since the topic of my Ph.D. thesis is The Use of Reconfigurable Architectures in Computer Networks, within the essay for the course Modern Theoretical Computer Science I describe some theoretical aspects related to partial dynamic reconfiguration (PDR) of the FPGA. We cannot see any model known from theory of formal languages behind the process of PDR itself, but its usage is always connected with solving a well-known optimization problem – the strip packing problem. Therefore, the aim of my essay is to show computational complexity of this problem and to provide a proof of it.

When partial reconfiguration of the FPGA is applied, functionality of some part of an implemented system is changed, while the rest of the system is untouched and still working. Since the whole partial reconfiguration process is done during the system runtime, we refer to it as partial dynamic reconfiguration. It is clear that for applying a mechanism of PDR, we have to be able to divide the whole system into a set of subsystems which we further refer to as tasks. Moreover, the set of tasks has to have two additional features: 1) implementation of all tasks together would exceed resources available in the FPGA and 2) some tasks can be multiplexed on the same FPGA resources in time.

A problem of placing a set of rectangles with some width and height on a strip with given width and unlimited height in such a way, that the height of an occupied part of the strip is minimal, is called the strip packing problem. We map the problem of scheduling tasks for PDR onto the strip packing problem in the following way. The set of rectangles represents the set of tasks, where the width of a rectangle corresponds to the number of occupied frames (the smallest reconfigurable unit of the FPGA) and its height corresponds to task processing time. Similarly, the width of the strip corresponds to the number of frames in the FPGA and its height represents time.

The above described mapping of time-multiplexed use of the FPGA resources onto the strip packing problem is usually exdended by a set of contraints specifying task arrival time (i.e. the earliest moment when the task can start) and a task deadline (i.e. the latest moment when the task must be finished). If we know all these parameters before the process of PDR starts, we are dealing with a so called offline strip packing problem and we can schedule all the tasks before the system is activated. The offline strip packing problem is NP-hard and the proof of this computational complexity is provided within the essay.

Even though an optimal solution of the offline strip packing problem cannot be determined in polynomial time with respect to the size of an input, we have to be able to find at least a suboptimal solution of this problem. Because of that, a number of heuristics have been developed for solving this problem. Some of them are briefly presented in the essay.