TLV3604, TLV3605 800-ps High-Speed RRI Comparator with LVDS Outputs

1 Features

- Low propagation delay: 800 ps
- Low overdrive dispersion: 450 ps
- High toggle frequency: 1.5 GHz / 3.0 Gbps
- Narrow pulse width detection capability: 600 ps
- LVDS output
- Supply range: 2.4 V to 5.5 V
- Input common-mode range extends 200 mV beyond both rails
- Low input offset voltage: ±5 mV
- Packages: 6-Pin SC70, 12-Pin QFN (3 mm × 3 mm)

2 Applications

- Distance sensing in LIDAR
- Time-of-Flight sensors
- High speed trigger function in oscilloscope and logic analyzer
- High speed differential line receiver
- Drone vision

3 Description

The TLV3604 and TLV3605 are 800-ps high speed comparators with a wide power supply range, rail-to-rail inputs, and a very high toggle frequency of 1.5 GHz. These devices also have exceptional overdrive dispersion performance of 450 ps. All of these features come in industry-standard small packages, making this device an excellent choice for LIDAR and differential line receiver applications.

The LVDS output helps increase data throughput, optimizes power consumption, and reduces EMI. It can directly interface most prevailing FPGAs and CPUs downstream in an application.

The TLV3604 is in a tiny 6 pin SC-70 package, which makes it easier for space sensitive applications such as an optical sensor module. The TLV3605 maintains the same performance as the TLV3604, and also offers adjustable hysteresis control, shutdown, and latching features in a 12 pin QFN package.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TLV3604	SC70 (6)	1.25 mm × 2.00 mm
TLV3605(2)	QFN (12)	3.00 mm × 3.00 mm

1. For all orderable packages, see the orderable addendum at the end of the datasheet.

2. For informational purposes only.

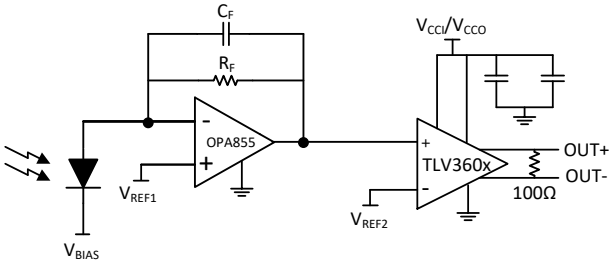

Figure 3-1. Optical Receiver Application

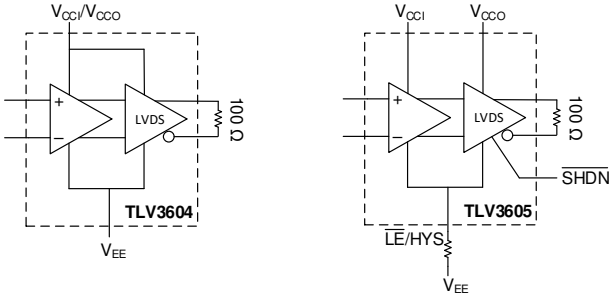

Figure 3-2. Functional Block Diagram

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Changes from Revision * (August 2020) to Revision A (August 2020)	Page
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5 Pin Configuration and Functions

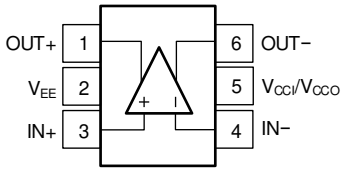

Figure 5-1. DCK Package, 6-Pin SC70, Top View

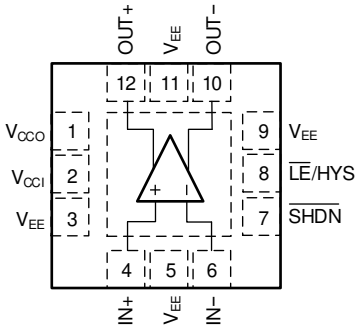

Figure 5-2. RVK Package, 12-Pin QFN, Top View

Pin Functions

PIN			I/O	DESCRIPTION
NAME	TLV3604	TLV3605		
IN+	3	4	I	Non-inverting input
IN–	4	6	I	Inverting input
OUT+	1	12	O	Non-inverting input
OUT–	6	10	O	Inverting output
V_{EE}	2	3, 5, 9, 11	I	Negative power supply
V_{CCI}	5	2	I	Positive input section power supply
V_{CCO}	5	1	I	Positive output section power supply
$\overline{SHDN}$	-	7	I	Shutdown control, active low
$\overline{LE}$/HYS	-	8	I	Adjustable hysteresis control and latch

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input Supply Voltage: $V_{CCI} – V_{EE}$	–0.3	5.5	V
Output Supply Voltage: $V_{CCO} – V_{EE}$	–0.3	5.5	V
Supply Voltage Difference: $V_{CCI} – V_{CCO}$	–5.5	5.5	V
Input Voltage (IN+, IN–)(2)	V_{EE} – 0.3	V_{CCI} + 0.3	V
Differential Input Voltage (V_{DI} = IN+, IN–)	–(V_{CCI} + 0.3)	+(V_{CCI} + 0.3)	V
Output Voltage (OUT+, OUT–)(3)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Shutdown Enable ($\overline{SHDN}$)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Current into Input pins (IN+, IN–, $\overline{SHDN}$, $\overline{LE}$/HYS)(2)	–10	+10	mA
Current into Output pins (OUT+, OUT–)(3)	–10	+10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.

(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM -TLV3604 only), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM -TLV3604 only), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standaed ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Supply Voltage: $V_{CCI} – V_{EE}$	2.4	5.5	V
Output Supply Voltage: $V_{CCO} – V_{EE}$	2.4	5.5	V
Input Voltage Range (IN+, IN–)	V_{EE} – 0.3	V_{CCI} + 0.3	V
Shutdown Enable ($\overline{SHDN}$)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC		TLV3604 DCK (SC70) 6 PINS	TLV3605 RVK (WQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.3	85.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	134.5	71.6	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	52.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.3	15.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	43.7	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.1	52.7	°C/W

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6.5 Electrical Characteristics (VCCI = VCCO = 2.5 V to 5 V)

V_{CCI} = V_{CCO} = 2.5 to 5 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, R_{LOAD} = 100 Ω, C_L = 1 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input offset voltage	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	-5	±0.5	5	mV
V_{CM}	Input common mode voltage range	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	V_{EE} – 0.2		V_{CCI} + 0.2	V
V_{HYST}	Input hysteresis voltage			0		mV
C_{IN}	Input capacitance			1		pF
R_{DM}	Input differential mode resistance			67		kΩ
R_{CM}	Input common mode resistance			342		kΩ
I_B	Input bias current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	-5	-1	5	uA
I_{OS}	Input offset current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	-1		1	uA
CMRR	Common-mode rejection ratio	V_{CCI} = V_{CCO} = 2.5 V and 5 V V_{CM} = V_{EE} – 0.2V to V_{CCI} + 0.2V, T_A = –40°C to +125°C	50	80		dB
PSRR	Power-supply rejection ratio	V_{CCI} = V_{CCO} = 2.4 to 5.5V, T_A = –40°C to +125°C	55	80		dB
DC Output Characteristics						
V_{OCM}	Output common mode voltage	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	1.125	1.2	1.375	V
ΔV_{OCM}	Output common mode voltage mismatch	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			20	mV
V_{OCM_PP}	Peak-to-Peak output common mode voltage			20		mVpp
V_{OD}	Differential output voltage	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	250	350	450	mV
ΔV_{OD}	Differential output voltage mismatch	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			10	mV
Power Supply						
I_{CC} (TLV3604)	Total quiescent current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C		12	16.5	mA
I_{CCI} (TLV3605)	Input stage quiescent current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C		7.5	10	mA
I_{CCO} (TLV3605)	Output stage quiescent current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C		5.2	7.0	mA
AC Characteristics						
t_{PD} (TLV3604)	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV, 50 MHz Squarewave		800		ps
t_{PD} (TLV3605)	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV, 50 MHz Squarewave		850		ps
t_{PD_SKEW}	Propagation delay skew	VOVERDRIVE = VUNDERDRIVE = 50mV, 50 MHz Squarewave		40		ps
$t_{CM\_DISPERSION}$	Common dispersion	V_{CM} varied from V_{EE} to V_{CCI}		200		ps
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 10 mV to 250 mV		450		ps
$t_{UD\_DISPERSION}$	Underdrive dispersion	Underdrive varied from 10mV to 250 mV		450		ps
t_R	Rise time	20% to 80%		350		ps
t_F	Fall time	80% to 20%		350		ps

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V_{CCI} = V_{CCO} = 2.5 to 5 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, R_{LOAD} = 100 Ω, C_L = 1 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		1.5		GHz
TR	Toggle Rate	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		3.0		Gbps
PulseWidth	Minimum allowed input pulse width	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV PW_{OUT} = 90% of PW_{IN}		600		ps
Latching/Adjustable Hysteresis (TLV3605 only)						
V_{HYST}	Input hysteresis voltage	R_{HYST} = Floating		0		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 150 kΩ		30		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 56 kΩ		60		mV
V_{IH_LE}	$\overline{LE}$ pin input high level	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	1.5			V
V_{IL_LE}	$\overline{LE}$ pin input low level	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			0.35	V
t_{SETUP}	Latch setup time			–3		ns
t_{HOLD}	Latch hold time			4.5		ns
t_{PL}	Latch to Q and $\overline{Q}$ delay			4		ns
Shutdown Characteristics (TLV3605 only)						
V_{IH_SD}	$\overline{SHDN}$ pin input high level	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	1.5			V
V_{IL_SD}	$\overline{SHDN}$ pin input low level	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			0.4	V
I_{IH_SD}	$\overline{SHDN}$ pin input leakage current	V_{CCI} = V_{CCO} = 2.5 V and 5 V V_{SD} = V_{CCO}, T_A = –40°C to +125°C			2	uA
I_{CCI_SD}	Input stage quiescent current in Shutdown mode	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			1.5	mA
I_{CCO_SD}	Output stage quiescent current in Shutdown mode	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			100	uA
t_{SLEEP}	Sleep time from Active to Shutdown mode	10% output swing		8		ns
t_{WAKEUP}	Wake up time from Shutdown mode	V_{OD} = 50 mV, output valid		100		ns

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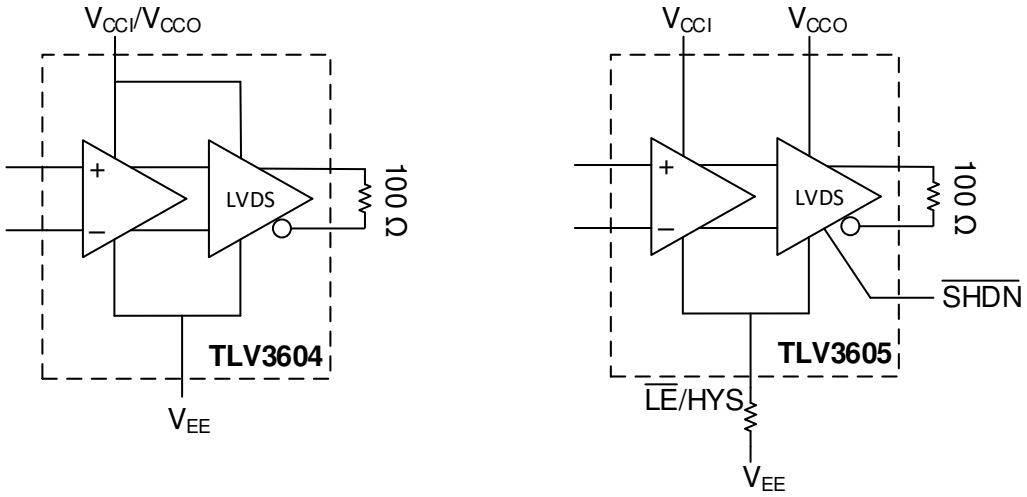
7 Detailed Description

7.1 Overview

The TLV3604 and TLV3605 are 800 ps propagation delay and 3.0 Gbps (1.5 GHz) comparators with LVDS output. The TLV3604 is ideally suited for time-of-light application, while TLV3605 is ideal for signal rectification and restoration with enhanced features. The TLV3604 is in the 6-pin SC-70 and TLV3605 is in 12-pin QFN package.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV3604 and TLV3605 are single channel, high speed with a typical propagation delay of 800 ps, LVDS output comparators. The minimum pulse width detection capability is 800 ps and the typical toggle rate is 3.0 Gbps. These comparators are ideal for time-of-flight as well as signal rectification type of applications. The rail-to-rail input stage capable of operating up to 200 mV beyond each power supply rail combined with a maximum 5 mV input offset without hysteresis gives 61 dB input dynamic range over the entire temperature range. The TLV3605 also provides shutdown enable and adjustable hysteresis controls. An external resistor can be used to configure the input hysteresis, making it immune to noisy environment.

7.4 Device Functional Modes

The TLV3604 has a single functional mode and is operational when the power supply voltage is greater than 2.3V. The TLV3605 has active mode and shutdown mode when power supply voltage is greater than 2.3 V. The TLV3605 is in shutdown mode when the $\overline{\text{SHDN}}$ pin is less than 0.4 V and is in active mode when $\overline{\text{SHDN}}$ pin is greater than 1.5 V. The $\overline{\text{SHDN}}$ is 1.8 V logic compliant and independent of power supply.

7.4.1 Rail-to-Rail Inputs

The TLV3604 and TLV3605 feature an input stage capable of operating 0 –200 mV below negative power supply (ground) and 200 mV beyond the positive supply voltage, allowing for zero cross detection and maximizing input dynamic range given a certain power supply. 5 mV maximum input offset without internal hysteresis in TLV3604 allows high sensitivity signal detection.

7.4.2 LVDS Output

The TLV3604 and TLV3605 output are LVDS compliant. When the input of the downstream device is terminated with a 100 Ω resistor, it provides a ±350 mV LVDS swing. Fully differential outputs enable fast digital toggling and reduce EMI compared to single-ended output standard.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV360x comparators feature rail-to-rail inputs and outputs on supply voltages as low as 2.4 V. The LVDS output stage is optimal for high speed applications that require low power consumption. The 850 ps propagation delay of the device makes it a suitable fit for applications involving optical reception, triggers for test and measurement systems, and transceiver type applications that require a high speed signal to be carried over a certain distance.

8.1.1 Comparator Inputs

The TLV360x is a rail-to-rail input comparator, with an input common-mode range that exceeds the supply rails by 200 mV for both positive and negative supplies.

8.1.2 Capacitive Loads

Under reasonable capacitive loads, the device maintains specified propagation delay. However, excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

8.1.3 Latch Functionality

The latch pin of the TLV3605 holds the output state of the device when the LE/HYST pin is less than 800mV above V_{EE}.

Figure 8-1, Figure 8-2 and Figure 8-3 illustrate proper latch timing for the device. Latch hold time is defined as the amount of time after the latch pin is asserted in which the input signal must remain stable (not force output toggle) in order to hold the proper output state at the time the latch pin was asserted. Latch setup time is the amount of time the input should be stable before the latch pin is asserted low. Figure 8-1 illustrates the amount of setup time needed for the output to properly latch an input state change. Figure 8-2 shows a proper amount of setup and hold time for a short input pulse when the latch pin is asserted such that the output latches the correct state. Figure 8-3 shows the timing diagram for when the latch pin is asserted high, and the time it takes for the output to properly unlatch.

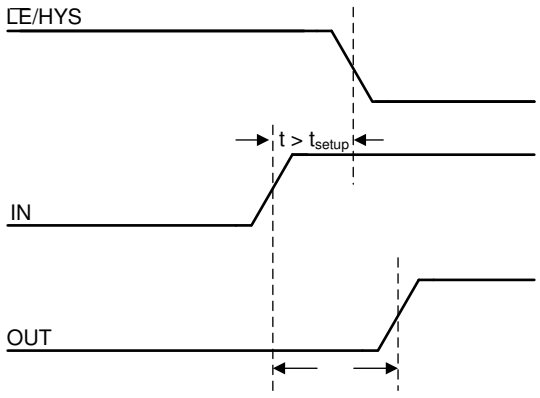


Figure 8-1. Input Change Properly Latched

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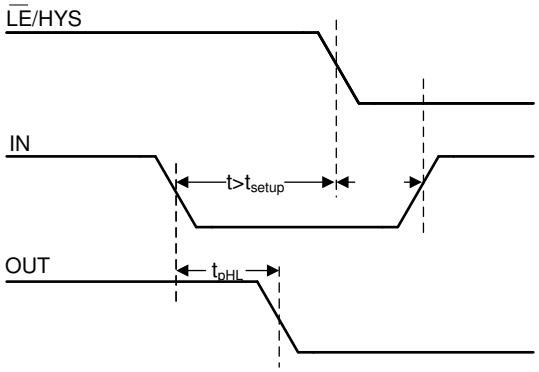

Figure 8-2. Short Input Pulse Properly Latched

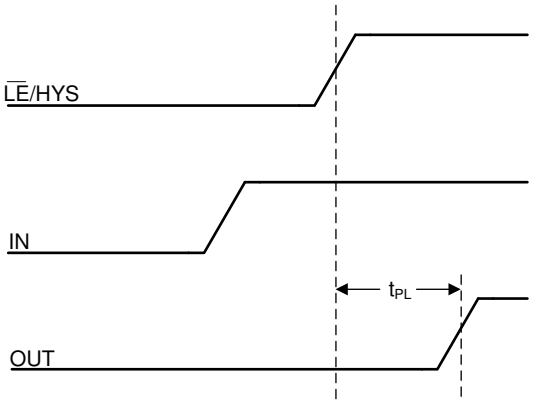

Figure 8-3. Latch Disable with Input Change

8.1.4 Adjustable Hysteresis

Because of a comparator's high open loop gain, there is a small band of input differential voltage where the output can toggle back and forth between a "logic high" and a "logic low". A clean input signal with fast slopes can pass this band quickly without problems. For slower and noisier signal slopes however, passing this band may cause the comparator output to switch back and forth between a "logic high" and a "logic low".

This issue can be addressed by hysteresis, which is a positive feedback loop that adjusts the trip point of the comparator depending on its current output state. The TLV3604 by default does not have any internal hysteresis.

The TLV3605 has a LE/HYST pin that can be used to increase the internal hysteresis of the part. The LE/HYST pin on this device can be modeled as a 1.25V voltage source in series with a 40k resistor. To change the internal hysteresis of the comparator, connect a single resistor as shown in the Figure 8-4 between the LE/HYST pin and VEE. When this resistor is left floating, the device will have 0mV of internal hysteresis.

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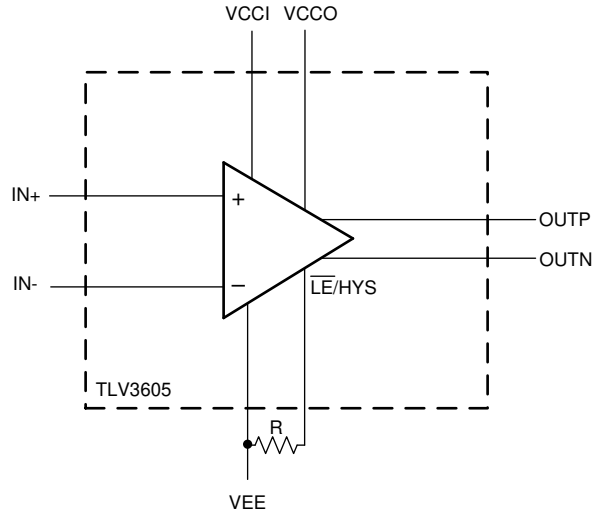

Figure 8-4. Adjusting Hysteresis with an External Resistor (R)

8.2 Typical Application

8.2.1 Optical Receiver

The TLV360x can be used in conjunction with a high performance amplifier such as the OPA855 to create an optical receiver as shown in the Figure 8-5. The photodiode is connected to a bias voltage and is being driven with a pulsed laser. The OPA855 takes the current conducting through the diode and translates it into a voltage for a high speed comparator to detect. The TLV360x will then output the proper LVDS signal according to the threshold set (V_{REF2}).

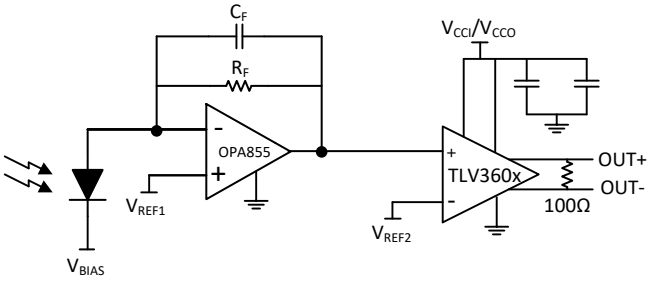

Figure 8-5. Optical Receiver

8.2.2 Logic Clock Source to LVDS Transceiver

The Figure 8-6 shows a logic clock source being terminated and driven with the TLV360x across a CAT6 Cable to receive an equivalent LVDS clock signal at the receiver end.

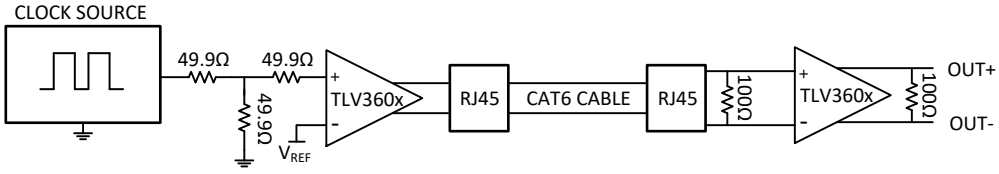

Figure 8-6. LVDS Clock Transceiver

8.2.3 External Trigger Function for Oscilloscopes

Figure 8-7 is a typical configuration for creating an external trigger on oscilliscopes. The user adjusts the trigger level, and a DAC converts this trigger level to a voltage the TLV360x can use as a reference. The input voltage from an oscilloscope channel is then compared to the trigger reference voltage, and the TLV360x sends an LVDS signal to a downstream FPGA to begin a capture.

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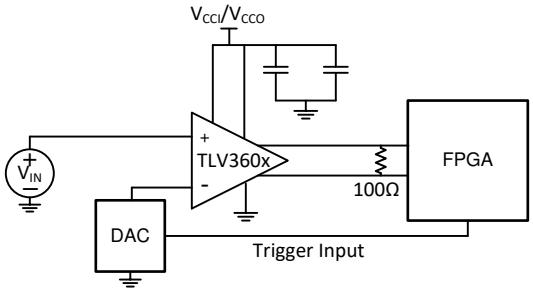


Figure 8-7. External Trigger Function

9 Power Supply Recommendations

The TLV3604 and TLV3605 is specified for operation from 2.4 V to 5.5 V. The TLV3604 and TLV3605 can operate on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Many specifications apply from –40°C to 125°C.

10 Layout

10.1 Layout Guidelines

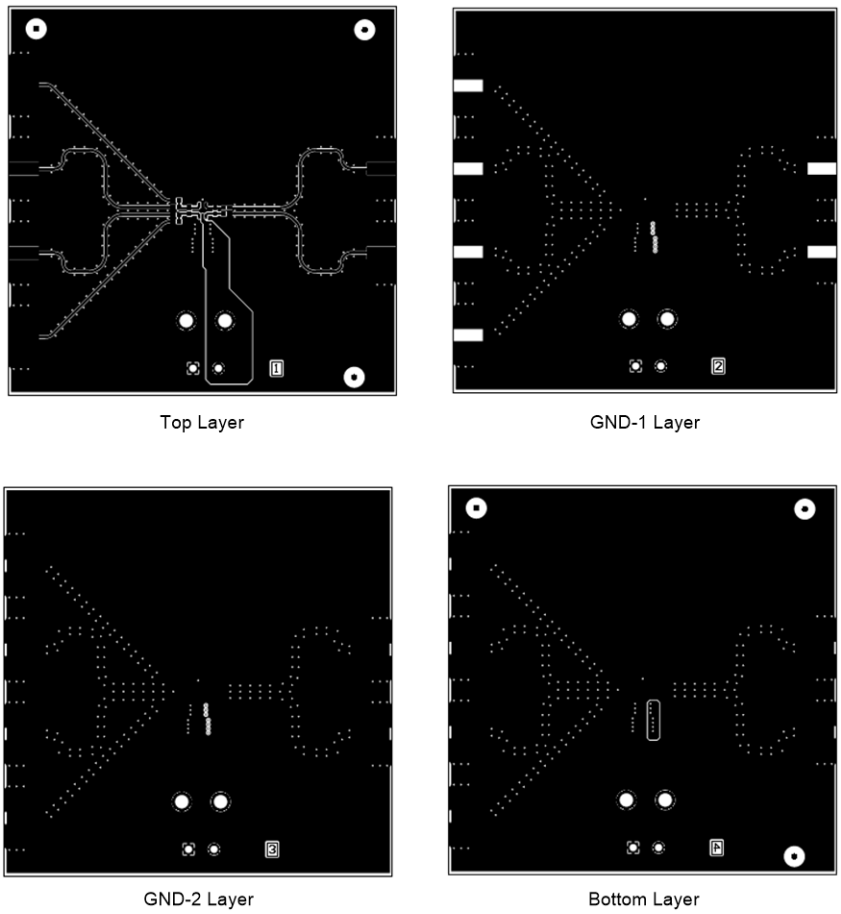
Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.
2. To minimize supply noise, place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when impedance is low. The topside ground plane runs between the output and inputs.
6. Use a 100 Ω termination resistor across the device's LVDS output.
7. Use higher performance substrate materials such as Rogers.
8. Below is the pcb signal layers from the TLV3604EVM as reference:

10.2 Layout Example

Figure 10-1 shows the 4 layer pcb signal routing for the TLV3604EVM as an example for how layout on this device can be done.

TLV3604EVM Layout Example



Top Layer

GND-1 Layer

GND-2 Layer

Bottom Layer

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LIDAR Pulsed Time of Flight Reference Design

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV3604DCKT	ACTIVE	SC70	DCK	6	250	TBD	Call TI	Call TI	-40 to 125		Samples
TLV3604DCKR	PREVIEW	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HF	
TLV3604DCKT	PREVIEW	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HF	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

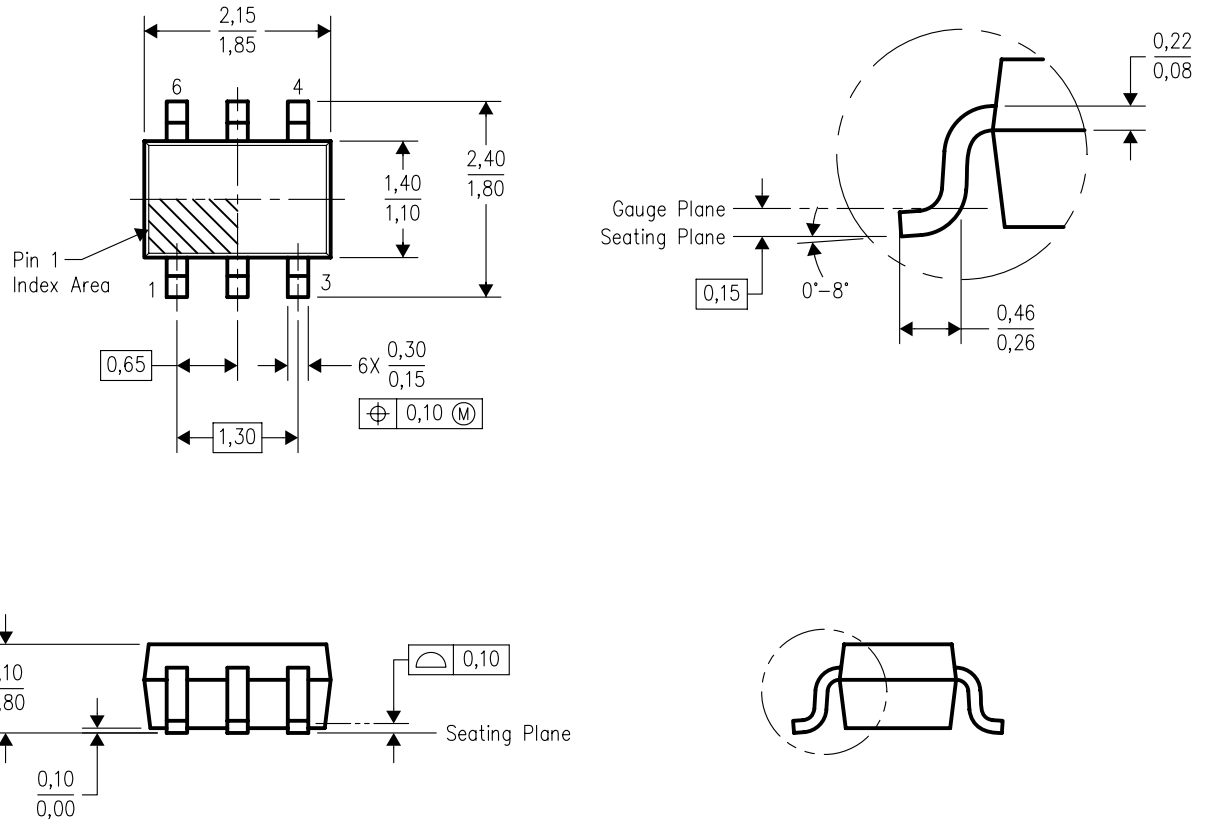
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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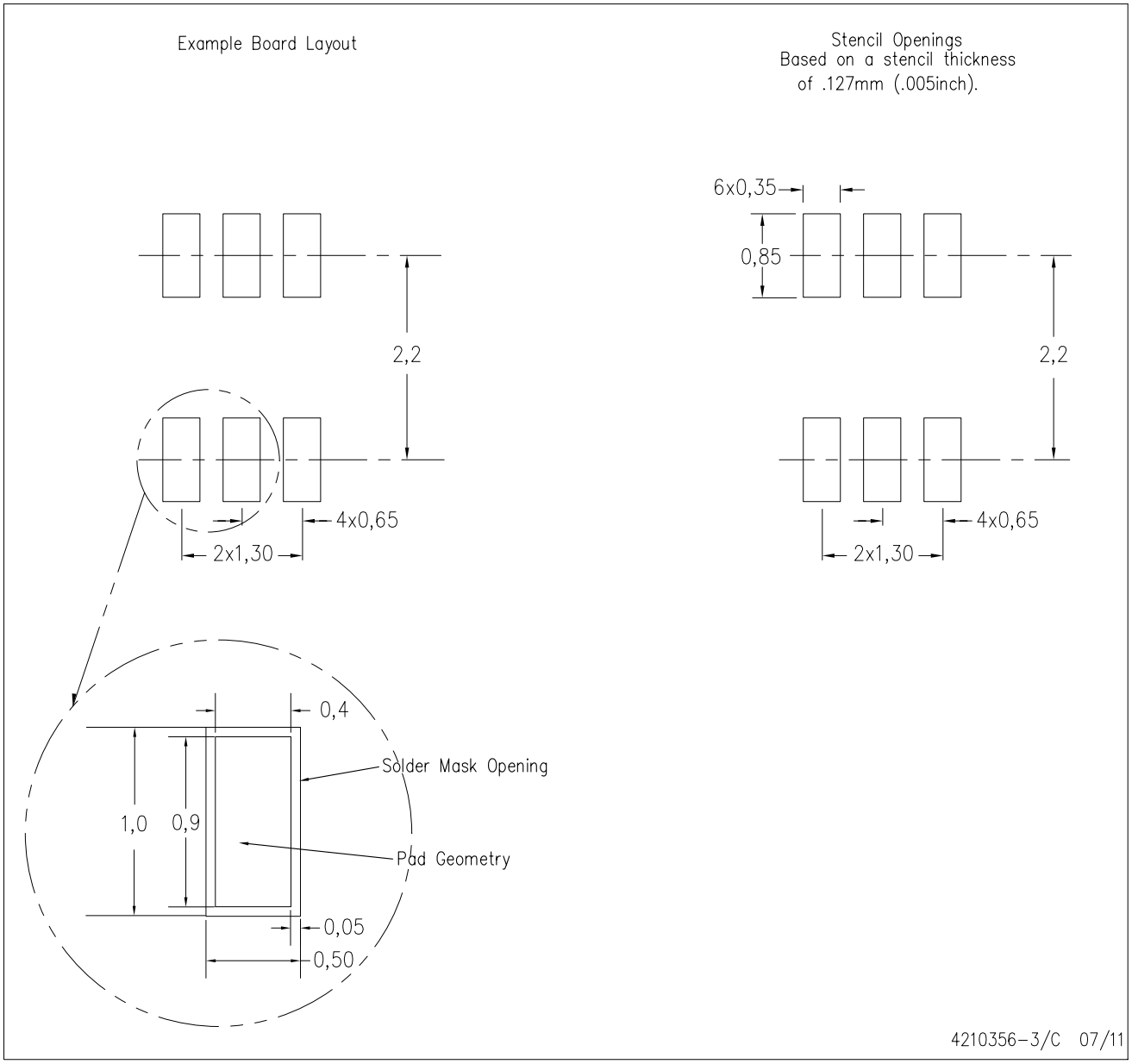
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265