

Evolutionary Design of Large Approximate Adders Optimized for Various Error Criteria

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ABSTRACT

As a promising approach to the design of energy efficient circuits, approximate circuits and approximate circuit design methodologies have attracted a significant attention of researchers as well as industry. Compared to the traditional design methods, it has been demonstrated that evolutionary approaches are able to discover approximate circuits exhibiting a good trade-off between the energy consumption and circuit quality. In this work, evolutionary design of large approximate adders is addressed. In order to improve scalability, the quality of the candidate solutions is analyzed using a formal approach based on Binary Decision Diagrams. Compared to the common approach based on a parallel circuit simulator, the proposed method is able to evaluate 2-3 orders of magnitude more generations.

CCS CONCEPTS

• **Computing methodologies** → **Search methodologies**; • **Theory of computation**;

KEYWORDS

Approximate computing, genetic algorithm, equivalence checking

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1 INTRODUCTION

With the growing interest in the use of various portable devices for monitoring and data processing, the semiconductor industry is facing several technology challenges. Among others, energy efficiency is one of the most prominent concerns driving both the industry and research community. Approximate computing is claimed to be an approach that promises significant efficiency gains at the cost of some quality degradation for applications that can tolerate inexactness in their output. There exist many applications

that are inherently error resilient, especially in the area of signal processing and machine learning.

Among others, various arithmetic circuits such as adders and multipliers have been approximated in literature [3]. Almost all circuit approximation methods compute the error by circuit simulation. An open question is how to obtain trustworthy results. Only a few papers deal with formal analysis of candidate approximate circuits to establish the error and provide formal guarantees on the error bound. Among others, the approximation of arithmetic circuits using Cartesian Genetic Programming (CGP) was addressed recently [1]. There are many error metrics that can be employed to evaluate the error of a candidate arithmetic circuit [2]. Despite of that, the authors typically deal with the worst-case error only because checking the worst error can be performed relative quickly using satisfiability solvers.

2 THE PROPOSED METHOD

In the context of the evolutionary design of digital circuits, the methods that evaluate the candidate solutions by applying a set of input vectors have been traditionally employed. Such approach, however, does not scale well because the number of vectors increases exponentially with the increasing number of inputs.

Recently, Reduced Ordered Binary Decision Diagrams (ROBDDs) were employed in the approximation of various benchmark circuits [5]. Vasicek et al. utilized a fitness function based on the average Hamming distance computed by means of BDD. The principle of the BDD-based approach is as follows. For each candidate solution, the absolute difference between the output of the accurate circuit and its approximation is calculated using a virtual circuit composed of the candidate and accurate circuits, subtractor and a circuit calculating absolute value. This circuit is then represented using BDD and analyzed. For a more detailed explanation, please see [5]. The main advantage of BDDs is that converting the virtual circuit to corresponding BDD and performing the error computation can be performed relatively quickly for many circuits relevant to practice.

In the context of a different design problem (optimization of BDDs), Soeken et al. proposed a BDD-based algorithm for determining the average arithmetic error, worst error and error rate [4]. The evaluation, however, included neither the adders nor the multipliers. In this paper, we propose to combine CGP with the BDD-based metrics and evaluate performance of the resulting method in design of approximate adders using CGP under different error criteria. The fitness is determined as the number of gates that a given candidate circuit contains. The error is used as a design constraint. If the error violates the predefined bound, the candidate solution is discarded.

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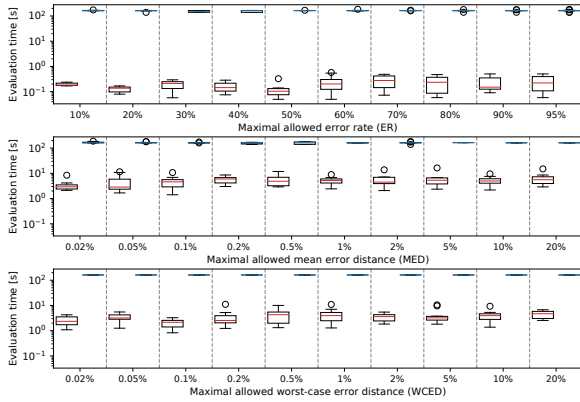


Figure 1: Time needed to perform the error analysis of 16-bit approximate adders using an optimized parallel simulator (blue) and the proposed BDD-based approach (red).

Three error metrics are considered – error rate (ER), mean error distance (MED) and worst-case error distance (WCED).

3 RESULTS

The performance of the proposed method was evaluated on the design of w -bit unsigned approximate adders, where $8 \leq w \leq 16$. The goal of the EA was to design the most compact approximate adder for each w and predefined error level ϵ , where ϵ specifies the maximum acceptable error. For each error metric, 10 error levels typically addressed in the literature were chosen. CGP parameters were as follows: $\lambda = X$, $\Gamma = \{BUF, AND, OR, XOR, NAND, NOR, XNOR, 0, 1\}$. Up to 5 genes were mutated using the point mutation operator. The search was terminated after producing $5 \cdot 10^6$ generations or when time-limit (3,600 sec) was exceeded. For each setting 10 independent runs were executed.

The results of performance analysis of the BDD-based method calculating the error of approximate adders are shown in Figure 1. The results are compared with an optimized approach based on exhaustive simulation (a circuit simulator that evaluates 64 input vectors in parallel was employed). As the average time needed to evaluate the error using the circuit simulator depends predominantly on the number of input vectors (2^{32} for the 16-bit adder), we can observe a constant performance independent of the error level and chosen error metric. Even though the performance of BDD-based method varies with the error level and especially with the error metric, it performs significantly better compared to the simulation. It scales better (it is intractable to handle 18-bit adders using simulation) and hence provides speedup in 2-3 order in the magnitude (nearly 10^3 for ER; nearly 10^2 for MED and WCED).

The average speedup of the proposed method is summarized in Table 1 (mean and standard deviation are provided for each w). The averages are determined from all 160 evolutionary runs to obtain statistically significant results. As expected, the BDD-based method performs better for more complex circuits (adders having at least 10 bits, i.e. 20 inputs). Compared to the WCED and MAE, determining error rate seems to be easier.

The best-evolved adders were synthesized and relevant design parameters were obtained with Synopsys Design Compiler (45 nm process). Fig. ?? shows the quality of the discovered approximate adders expressed in terms of the achieved power reduction. The

Table 1: The speedup of the BDD-based method for error analysis of w -bit adders using three error metrics.

w	ER		MED		WCED		avg
	avg	stddev	avg	stddev	avg	stddev	
8	1.7	0.4	1.5	0.8	1.5	0.5	60.5
10	49.2	16.5	4.5	2.9	4.0	1.0	19.2
12	130.8	28.2	8.0	4.7	11.3	3.3	50.1
14	363.8	56.7	14.4	8.4	22.6	9.7	133.6
16	963.9	292.8	51.1	26.8	75.5	43.7	363.5

power reduction is given relatively to the accurate w -bit ripple carry adder. If WCED is constrained to 0.1, for example, power can be reduced to less than 60 % in case of 16-bit adder. There exists a relative strong dependency between the power consumption and the level of WCED (MED). In both cases, the power decreases with the increasing WCED (MED). The 20% error level leads to almost 99% power reduction. In the case of the error rate, the power reduction is moderate. In addition to that, it even decreases with increasing w . For 16-bit adder and 90% ER, for example, power dropped by 30% only. It seems that the chosen target error level is not sufficiently large to allow substantial power reduction. This result is worth to investigate not only from the theoretical point of view but also from the practical point of view because it can explain why the analytic adders exhibiting error rate around 80% provide moderate power savings [2]. When we analyzed the adders designed for WCED and MED, their error rate was 98.8% in the average even though the absolute error was low.

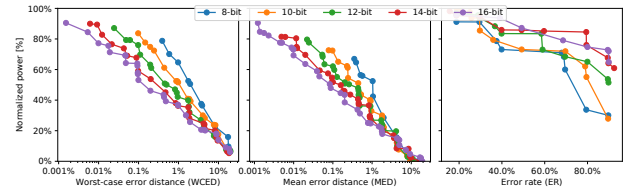


Figure 2: Power consumption of the approximate adders optimized for a particular error metric.

4 CONCLUSIONS

We adopted CGP where we replaced the common fitness function with a BDD-based approach for determining the quality of approximate adders. Compared to the common CGP, our approach enabled us to significantly accelerate the evolutionary design process and increase the quality of the evolved solutions. For 16-bit adders (i.e. 32-bit circuits), for example, 50x more evaluations was executed within the same amount of time.

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