Fault Tolerance in HLS for the Purposes of Reliable System Design Automation

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Abstract

Nowadays, many important processes are controlled by electronic systems. Nevertheless, if such system fails, the resulting damage might result in high economical loss or even endanger human health. As an example, autonomous vehicles, which are very popular these days, may serve. Another example might be a device that is possibly not serviceable for a very long period of time, such as a space probe or an artificial satellite. The reparation cost of these devices is well worth the effort to make these devices reliable as much as possible. This effort makes designers focus on the aspects of system reliability. Furthermore, as the chip-level integration grows, the resulting systems are increasingly prone to their failure, further increasing the importance of such aspect of reliability. The complexity of today's modern systems, however, makes this a difficult task to solve.

One possible solution to ensure higher reliability is to make a system so-called Fault Tolerant (FT), which means its ability to perform its function even during presence of faults. The system, however, still remains composed of non-reliable parts. Each method of FT is characterized by the way the non-reliable parts are composed to improve the overall reliability of the resulting system. The solution to the high complexity of today's systems is to move the development to a higher level of abstraction. High-Level Synthesis (HLS) is becoming popular for allowing further move to a higher level of abstraction. Using HLS it is possible to transfer an algorithm (e.g. described in a higher-level programming language, such as C++) to its Register Transfer Level (RTL) representation (e.g. described in a VHDL language).

Our research focuses on an combination of HLS and FT, as we believe the combination of these approaches solves both the problems. We developed an approach to insert reliability to HLS-generated systems. Many approaches to incorporate FT into HLS exist, however, in our approach, the input algorithm is modified *before* its processing by the HLS tool and, thus, the HLS tool itself does not require any modification. The descriptions of FT methods are then made on the same abstraction level as the language used to describe the algorithm, thus, making them easier to develop and maintain. The source algorithm is separated from the FT description making the code easier to maintain as well. The overview of this approach is shown in Figure 1.

In the presentation, this existing method to insert redundancy into HLS-generated systems will be briefly described alongside with its improvement in the form of a majority function selection. We found out that the type of the majority function affects not only the resulting reliability, but also the resources

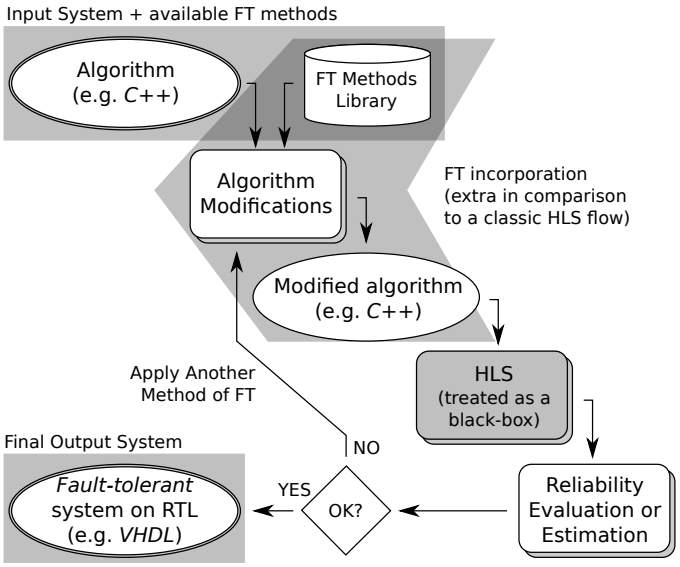

Figure 1: The approach to insert redundancy into systems generated using HLS.

consumption. The presentation also addresses the level of redundancy selection, as we evaluated various numbers of redundant modules with multiple fault occurrences. The case study experiments are carried out with our robot verification platform utilizing the so-called left-hand algorithm and fault injection into a Field Programmable Gate Array (FPGA) implementing the robot controller. This approach is not limited to FPGAs, however, we use an FPGA technology during the evaluation for its wide range of applications and its versatility.

Paper origin

The original paper has been accepted and presented at the 16th IEEE East-West Design & Test Symposium (EWDTS-2017) in Serbia [1].

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References

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