VIRTA: VIRTUAL PORT BASED REGISTER-TRANSFER LEVEL TESTABILITY ANALYSIS AND IMPROVEMENTS

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Abstract. *The work deals with testability analysis of data-path within register-transfer level digital circuits and with utilizing its results in selected areas in digital circuit diagnostics area. In the work, it is shown that it is advantageous if each module stored in a design library is equipped both with design-related information and special diagnostics-related information usable for testability-analysis purposes in our case. During our research, such information was described by means of a formal mathematical model based on so-called transparency conception. Proposed digraph-search based testability analysis method is described by means of instruments specified in the model.*

1 Introduction

To be able both to satisfy design constraints posed on a digital circuit and to ensure acceptable testability of the circuit, a design tool is required to be informed about the quality (in view of testability parameters and level of satisfaction of design constraints) of a particular solution to the circuit design. Such information can be provided, e.g., by a *testability analysis* method. At present, exact (standardized) definition of testability does not exist. Generally, testability is understood as a characteristic involving various costs related to digital circuit testing. However, differences in existing testability definitions lead to various understanding of some testability related concepts, components and consequently of measures used for testability evaluation. Most of those drawbacks should disappear after unification of actual testability definitions into one standardized definition that is planed to be involved in IEEE P1522 standard [5]. Existing testability analysis methods can be sectioned to gate-level methods (e.g., SCOAP, TMEAS), RTL methods (e.g., TMEAS, CAMELOT, COPS, STA, ITA), high-level methods (e.g. SATAN, FACTOR) and multi-level methods.

In the paper, ideas and application results of a new *register-transfer level* (*RTL*) testability analysis method are presented. There are two groups in the area of RTL testability analysis methods. Methods from the first group are based on a probability model of a diagnostic data flow through modules (i.e., elementary sub-circuits stored in a design library) within the circuit structure. For each module, several probability-characteristics exist determining probability of a certain input-output data-transfer of each module-type. Methods from the second group are based on a model of selected diagnostic properties of circuit modules. Property-based models allow diagnostic data flow to be modeled more precisely and in more detail, but they are more complex in general. As testability analysis method is inspired by a certain test-generation principle [8], results of the first-group methods are practically applicable when a pseudorandom test generator is to be used. Results of the second-group methods are more general, and thus applicable when deterministic test generator is to be used or combined with pseudorandom or other test generation method. Work presented in this paper is related to the methods belonging to the second group and deals only with the problem of testability of a data-path that utilizes a multiplexed data-path strategy for data-flow switching in RTL digital circuits. The paper is organ-

ized as follows. First, research motivation in testability analysis area is presented, then our research activities including our research goals, principles of proposed solution and method analysis results are summarized. At the end of the paper, experimental results together with comparison with existing approaches, conclusions and future trends are given.

2 Our Research Activities

During our research, previous model [1, 3] of RTL circuit data-path and of *I-path* transparency concept was extended. *I-path* concept supposes *n*-bit diagnostic data transfer is possible between port *x* and *y* iff both *x* and *y* are *n*-bit ports and each *n*-bit data can be transferred unchanged in the direction from *x* to *y* (i.e., one-to-one identity mapping exists between *x*-data and *y*-data). In Fig. 1, example of modules *I-path* concept can be used to model their diagnostic properties is presented.

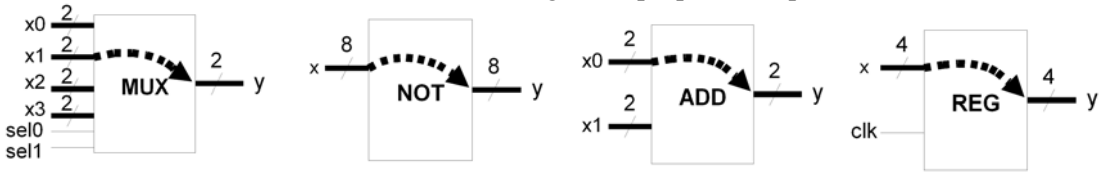

Figure 1: Illustration to *I-path* concept

In Fig. 2, module *M* that is not able to use the *I-path* concept for modeling diagnostic data transfer through its structure is presented. In the module, two ports with the same bit-width don't exist, thus it is impossible to describe diagnostics data transfer using *I-path* concept. However, as can be seen in tables d) to h), due to existence of several "partial" mappings, it is possible to transfer "partial" diagnostic data through the structure of *M*. From this point of view, module seen as a module "disabling transfer of a diagnostic data" using *I-path* conception can be seen as "partially suitable" for the same purpose using more general transparency conception. It can be seen that accuracy of data-path analysis strongly depends on used transparency model.

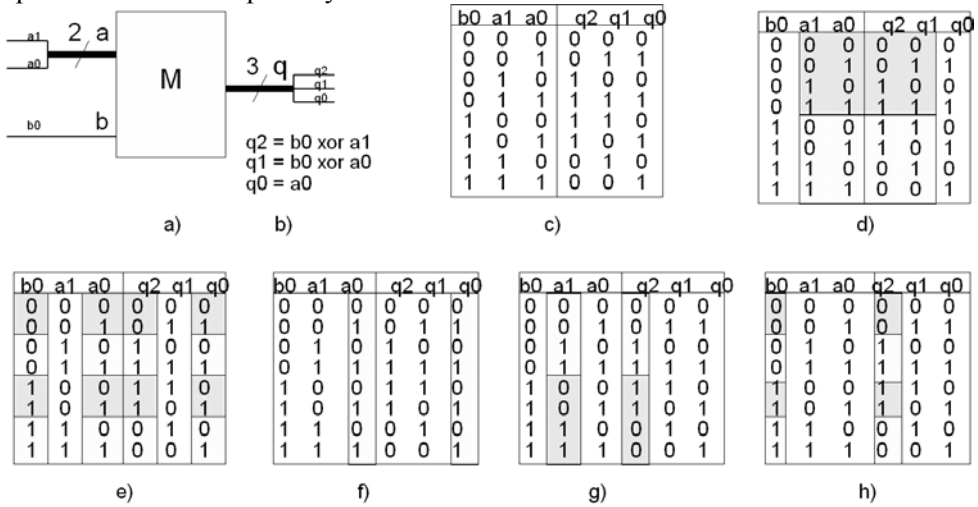

Figure 2: Illustration to transparency modes based on virtual port concept

Our research results show it is not necessary to require existence of one-to-one identity mapping between *x*-data and *y*-data nor existence of one-to-one mapping between *x*-data and *y*-data to be able to model diagnostic data transfer through module structure; such a requirement is too strict and leads to unneeded restriction of set of data-paths suitable for transferring diagnostic data. During our research, it was also shown that it is advantageous to analyze circuit data-path separately for transferring test vectors and responses: 1) test vectors can be transferred through a module structure iff a surjection exists between data at a module port *x* and a module port *y*, 2) responses can be transferred through a module structure iff an injection exists between data at a module port *x* and a module port *y*.

In our approach, transparent data-paths suitable for transferring diagnostic data are considered between so called *virtual ports*. Virtual port abstracts from the designer-defined module interface and

can be understood as a generalized port forming the interface. Let us give some example of what virtual port means. In Fig. 2, module M is presented. Its designer-defined interface consists of input ports $a = (a_1, a_0)$, $b = (b_0)$ and output port $q = (q_2, q_1, q_0)$. Set of all virtual input ports of M (i.e., set $VPORT_M$) consists of a subset of $\{a_1, a_0, b_0\}^+$ and set of all virtual output ports is a subset of $\{q_2, q_1, q_0\}^+$. Each a subset consists of unordered n-tuples including each element at most once. Using virtual ports, it is easy to describe existence of "partial" mappings between data at module inputs and module outputs, especially to describe proposed principles and algorithms. Over virtual port sets, range of instruments is defined. The instruments can be divided to *circuit structure modeling instruments* (giving information about in-circuit modules, their types, interfaces, operation modes, interface connections, data-flow etc.) and to *transparency conception modeling instruments* (especially over-$VPORT_{CUA}$-set relations giving information about diagnostics data-flow through in-circuit modules structure). Having information about how interfaces of various modules are interconnected and information about diagnostic-usable mappings between virtual ports within the circuit, it is possible to construct two special digraphs for the circuit: *test-pattern data-flow digraph* G_S and *test-response data-flow digraph* G_I. Vertices of G_S (G_I) are virtual ports; an oriented edge exist between two vertices iff surjection (injection) exists between the start-vertex and end-vertex data, i.e., iff it is possible to transfer test-vectors (responses) from start-vertex to end-vertex. Pairs of vertices that a test-vector (response) data flow is possible between them, together with information about required flow-condition are put in special relations that form a basis for constructing edges of G_S (G_I). Proposed testability analysis algorithm is constructed as a graph-searching algorithm performing node-accessibility analysis over G_S and G_I. During the search process, accessibility of virtual ports from circuit primary inputs (controllability analysis) is analyzed in G_S and accessibility of virtual ports at circuit primary outputs (observability analysis) is analyzed in G_I. Evaluation of x-controllability can be understood as evaluation of "easiness of controlling values at x by means of stimuli generated at circuit primary inputs". Alike, evaluation of x-observability can be understood as evaluation of "easiness of observing values at x by means of circuit primary outputs". Because x is understood as testable if it is both controllable and observable, evaluation of testability is a function of controllability and observability. Some of important properties of proposed testability analysis algorithm were proven -especially proof of algorithm correctness (i.e., that the algorithm finds all accessible vertices that they are accessible and that the more accessible vertex is evaluated worse than the better accessible one) and proof of algorithm time complexity-it was proven that the algorithm runs in $O(|V(G_S)|\cdot|E(G_S)| + |V(G_I)|\cdot|E(G_I)|)$, where $V(G)$ is a set of vertices of G and $E(G)$ is a set of edges of G. Not enough space here for the algorithm.

3 Experimental Results

To experimentally prove some of algorithm properties, algorithm was implemented in C++ and applied on following benchmark circuits: *Bert*, *Diffeq*, *Paulin* and *Tseng* [2, 3, 6]. Their testability analysis results are presented in the following table. Each circuit is related with exactly one row in the table. The row informs (in left-to-right direction): 1) about the number of elementary data ports in the circuit, 2) about circuit controllability (ratio of controllable data ports), 3) about circuit observability (ratio of observable data ports) and 4) about circuit testability (ratio of testable data ports).

Table 1: Testability analysis results.

Circuit	# of data-ports	Con. (%)	Obs. (%)	Tst. (%)
Bert	440	0.943 (100)	0.765 (100)	0.721 (100)
Diffeq	400	0.423 (56)	0.173 (28)	0.073 (0)
Paulin	512	0.912 (100)	0.833 (100)	0.760 (100)
Tseng	360	0.921 (100)	0.847 (100)	0.780 (100)

There are two areas, where above-mentioned testability analysis method was applied. First area is the area dealing with generation of synthetic RTL benchmark circuits [4], second is a design for testability area. The method was used here to find a solution for the problem of selecting registers into scan chains. The goal was to select (a minimal number of) registers into scan chains and to chain them in such a way the highest possible testability of resulting design is achieved together with the lowest price proportional to size of modifications caused by scan application in the original circuit structure.

Results are presented in Table 2 and they are written using below-mentioned notation. Symbol '*' in a table cell means that an application of scan technique does not lead to desired testability improvement at given design constraints, symbol '-' means that the circuit was not analyzed by the method.

Table 2: Results of selecting registers into scan chains.

Tested method	**Scan-layout results of the method applied on benchmarks:**			
	Bert	*Diffeq*	*Paulin*	*Tseng*
[2]	$R_5R_4R_1R_2$	$R_4R_6R_1R_5$	-	R_5R_1
[3]	-	$R_1R_2R_4$	-	*
Proposed [6]	*	R_1R_6	*	*

During our previous research activities [7], problem of scan-layout state-space analysis and a formal notation for scan-layout description was solved. Let the notation be summarized in brief by following points: 1) scan chain is represented by a sequence of registers that are chained within the chain, 2) special character (period, dot) is used to separate particular scan chains, 3) if the ordering of scan registers within the scan chains is not important, registers belonging to the same scan chain are chained in the left-right direction according to increasing values of indexes (registers with higher indexes are placed on the right), 4) scan chains are ordered in a left-to-right way according to increasing index of the first register in a scan chain (chains with higher index of the first register are placed on the right), 5) if there is no register placed into scan, notation contains only special character.

4 Conclusions and Acknowledgements

Main subject of the work was to deal with a testability analysis of RTL digital circuit data-path and with utilizing its results in selected areas within the digital circuit diagnostics area. Main advantage of the approach presented in the paper can be seen in the possibility to utilize the greater part of data-path for diagnostic purposes in general. One of main contributions of this work can be seen in the possibility to transform testability analysis problem to a mathematical problem that can be solved as a graph-searching problem applied to so-called test-pattern data-flow digraph and then to so-called test-response data-flow digraph. Our experimental results show that due to a more detailed analysis of circuit data-path, proposed testability analysis method informs more precisely about circuit testability than existing methods do. This work has been financially supported by the Grant Agency of the Czech Republic under contract GA102/04/0737 "Modern Methods of Digital Systems Design" and contract GA102/05/P193 "Optimizing Methods in Digital Systems Diagnosis".

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