Review of the Dissertation Thesis

Thesis title: Mapping of Packet Processing from P4 Language to FPGA Technology
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Supervisor: doc. Ing. Jan Kořenek, Ph.D.
Reviewer: doc. Ing. Petr Fišer, Ph.D.

Thesis contribution

The Thesis proposes novel architectures for packet classification, targeted to high-speed networks (100 Gbps and more). The target technology is FPGA and the aim is to have the architectures configurable by the P4 language. Emphasis is put on scalability, flexibility, and memory efficiency.

The investigated topic is very timely without doubt. Network security is of a big concern for many years already, and becomes ever important. Moreover, networks speeds (throughputs) are constantly increasing and thus there is a need to develop faster and better network monitoring mechanisms, which are able to keep pace with this speed increase. Standard computers cannot be used for this purpose, because they are, simply, slow. Thus, specialized hardware must be designed. FPGAs offer great flexibility and ability to be reprogramed, when an update is needed. Thus, they are the best choice to serve this purpose.

Thesis structure

The Thesis is written as a collection of papers with a supporting text.
The Thesis is structured into four chapters as follows:

- Chapter 1 presents an introduction to the problematics and the objectives of the Thesis. Here I'm missing one of the main motivations: *why do we need the packet classification*? An unfamiliar reader may miss the very purpose of the work. Also, some other terms need not be generally known (e.g., the match/action table, dimension, etc.).
- Chapter 2 reviews the state-of-the-art, the principles of software-defined networks (SDNs), the P4 language, the packet classification problem, and finally the related work. I appreciate such a comprehensive summary of previous works.
- Chapter 3 reports the author's research progress and the final contributions. I think the research was conducted in a reasonable way, starting with the DCFL architecture and then improving it. Summaries of the author's papers are presented at the end of this chapter.
- Chapter 4 contains the final discussion and conclusions. The final experimental results are presented there as well.

The Thesis is well written, in a very good English, with a minimum of typos.

My comments

- As stated above, some essential terminology and principles are not introduced at the very beginning of the Thesis. Some terms (like the match/action table, dimension) are used before they are defined.
- Tab. 3.1 contains two equal rulesets. I suppose it is a typo.

Publication activity

The contributions of the Thesis were published in one impacted journal article and five reviewed international conference papers. In addition, there are also two related papers published in two reviewed conferences. From this, I'm judging the applicant's publication activity as sufficient.

Questions to the defense

- Are there any similar architectures you can compare with? I suppose this problem is being solved all over the world and probably by different means. Thus, are you aware of different architectures doing the same job?
- Why is the memory efficiency that important? As the architecture is being implemented in an FPGA, all available BRAMS can be freely used. In case of using external memory, I don't think its size is a bottleneck.
- How difficult would it be to port the architecture to ASIC? Since the rules are stored in external memory, I think it shouldn't be a big problem. And probably the throughput would be increased as well.

Final assessment

Judging from the above, it can be concluded that the applicant is scientifically qualified. He has proven the ability to conduct his own research and publish the results. Therefore,

I do recommend

the submitted thesis for the presentation and defense.

In Prague, 6. 5. 2024

doc. Ing. Petr Fišer, Ph.D.
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